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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,674	09/30/2003	Wendy Ann Belluomini	AUS920030494US1	6770

45992 7590 01/08/2007

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,674	BELLUOMINI ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006 and 30 September 2003 an*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *11-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-9 and 22* is/are rejected.

7)☒ Claim(s) *5-7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to the Response to Election/Restriction filed 10/23/2006.

2. Claims 1-22 are pending in this application. Claims 1, 11, 16, and 22 are independent claims. In the Response, claims 1-10 and 22 are elected with traverse and claims 11-21 are withdrawn from consideration. This Office Action is made non-final.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 22, drawn to a detail structure of a fused Booth encoder multiplexer logic cell, classified in class 708, subclass 625.

II. Claims 11-21, drawn to a multiplier circuit, classified in class 708, subclass 620.

The inventions are distinct, each from the other because of the following reasons:

4. Inventions of Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Group II drawn to a multiplier circuit does not require the particulars features of Group I drawn to a detail structure of a fused Booth encoder multiplexer logic cell. The

subcombination has separate utility such as the detail structure of a fused Booth encoder multiplex logic cell.

5. The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

6. Claims 11-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/23/2006.

7. Applicant's election with traverse of Group I claims 1-10 and 22 in the reply filed on 10/23/2006 is acknowledged. The traversal is on the ground(s) that both groups pertain to a fused Booth encoder multiplexer designed for a multiplier circuit. This is not found persuasive because:

> Regardless of both groups relating to a multiplier, Group I is clearly addressing only the individual of a fused Booth encoder multiplexer logic cell in a deep detail as structural connection of transistors as seen in Figures 4-6 whereas Group II is only briefly mentioned the fused Booth encoder multiplexer logic unit but focuses more in overall structural connection of multiplication unit as seen in Figure 8. In generally, the detail of

individual of a fused Booth encoder multiplexer logic cell as cited in Group I does not necessary required in the overall structural connection of multiplication unit as cited in Group II or vice versa.

The requirement is still deemed proper and is therefore made FINAL.

Specification

8. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

9. The abstract of the disclosure is objected to because the abstract is written more than 150 words in length.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 1, 3, and 22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Re claims 1, 3, and 22 cite a fused Booth encoder multiplexer logic cell that operates in accordance with a pre-defined mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result, regardless whether it is implemented in hardware or software. However, claims 1, 3, 22 are merely disclose a logical structure of a Booth encoder multiplexer without mentioning its practical/physical application or its useful and tangible result. The output of this Booth encoder multiplexer logic cell is just a partial product of inputted operands. Therefore, claims 1, 3, and 22 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-3 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art.

Re claim 1, the admitted prior art discloses in Figures 1-3 a fused Booth encoder multiplexer logic cell (e.g. corresponding to both Booth selector 14 and Booth encoder 12 in Figure 1 wherein each cell is logically represented in tables 1-2) comprising: a logic circuit (e.g. Figures 1-2 and page 4 of specification) having a plurality of operand input

bits (e.g. the input operand for Booth selector 14 is A and the input operand for Booth encoder 12 is C in Figure 1) including multiplier input bits (e.g. represent by C(I-1, I, I+1) in table 1) and multiplicand input bits (e.g. represent by A(I, I+1) in table 2), and an output node which produces a single partial product bit (e.g. output of table 2) according to a Boolean function of plurality of operand input bits based on a Booth encoding and selection algorithm (e.g. line 1 page 4 to line 5 page 5 of specification).

Re claim 2, the admitted prior art further discloses in Figures 1-3 the logic cells are arranged in a two-dimensional array on an integrated circuit and operate in parallel (e.g. Figure 2 and lines 12-20 page 4) to produce a respective plurality of partial product bits (e.g. each of three bits multiplier would yield a partial product according to tables 1-2 in pages 4-5 of specification); and a given one of the logic cells has a unique set of multiplicand and multiplier input bits (e.g. page 4 lines 1-12).

Re claim 3, the admitted prior art further discloses in Figures 1-3 the operand inputs bits include two multiplicand input bits A(i..i+1) and three multiplier input bits C(i-1..i+1); and the Boolean function which produces the single partial product bit is given by the expression S=(A(i).sym.C(i-1)).multidot.(C(i).sym.C(i+1))+A(i+1).multidot.{overscore (C(i-1))}.multidot.C(i).multidot.C(i+1)+{overscore (A(i+1))}.multidot.C(i-1).multidot.{overscore (C(i))}.multidot.{overscore (C(i+1))} (e.g. output of table 2 is done/outputted according to this expression).

Re claim 22, the admitted prior art discloses in Figures 1-3 logic circuit for a fused Booth encoder multiplexer logic cell (e.g. corresponding to both Booth selector 14

and Booth encoder 12 in Figure 1 wherein each cell is logically represented in tables 1-2), comprising: two multiplicand inputs A(i..i+1) (e.g. corresponding to A(1) and A(2) in table 2); three multiplier inputs C(i-1..i+1) (e.g. corresponding to three input bits of C in table 1); an output node; and a plurality of interconnected transistors controlled by multiplicand and multiplier inputs, respectively, transistors producing a value at output node such that (e.g. each of the result is composed of both tables 1 and 2 in pages 4-5 of original specification): the value is the first multiplicand input A(i) when the first multiplier input C(i-1) is on and when only one of the second and third multiplier inputs C(i..i+1) is on (e.g. corresponding to C(I-1, I, I+1) = 001 or 010 in table 1 yields result of A(1) in table 2); the value is the complement A(i) of the first multiplicand input when the first multiplier input C(i-1) is off and when only one of the second and third multiplier inputs C(i..i+1) is on (e.g. corresponding to C(I-1, I, I+1) = 101 or 110 in table 1 yields result of bar(A(1)) in table 2); the value is the second multiplicand input A(i+1) when the first multiplier input C(i-1) is off and when both of the second and third multiplier inputs C(i..i+1) are on (e.g. corresponding to C(I-1, I, I+1) = 011 in table 1 yields result of A(2) in table 2); the value is the complement {overscore (A(i+1))} of the second multiplicand input when the first multiplier input C(i-1) is on and both of the second and third multiplier inputs C(i..i+1) are off (e.g. corresponding to C(I-1, I, I+1) = 100 in table 1 yields result of bar(A(2)) in table 2); and the value is off when the multiplier bits C(i-1..i+1) are either all on or all off (e.g. corresponding to C(I-1, I, I+1) = 111 or 000 in table 1 yields result of 0 in table 2).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4 and 8-9 are rejected under 35 U.S.C. 103(a) as being obvious over the admitted prior art in view of Houston (U.S. 5,208,489).

Re claim 4, the admitted prior art fails to disclose in Figures 1-3 a clock input; a logic tree containing a plurality of logic transistors controlled respectively by plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node; a power transistor coupling logic tree to a voltage source, power transistor being controlled by clock input; a foot transistor coupling logic tree to electrical ground, foot transistor being controlled by clock input; and a latch connected to dynamic node which maintains the value at output node, latch being controlled by clock input. However, Houston discloses in Figures 1-12 a clock input (e.g. CLK in every Figures); a logic tree containing a plurality of logic transistors controlled respectively by plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node (e.g. col. 1 lines 17-25 and lines 40-45); a power transistor coupling logic tree to a voltage source, power transistor being controlled by clock input (e.g. transistor 194 in Figure 9a as an example only); a foot transistor coupling logic tree to electrical ground,

foot transistor being controlled by clock input (e.g. transistor 196 in Figure 9a as an example only); and a latch connected to dynamic node which maintains the value at output node, latch being controlled by clock input (e.g. area 126 in Figure 6). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a clock input; a logic tree containing a plurality of logic transistors controlled respectively by plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node; a power transistor coupling logic tree to a voltage source, power transistor being controlled by clock input; a foot transistor coupling logic tree to electrical ground, foot transistor being controlled by clock input; and a latch connected to dynamic node which maintains the value at output node, latch being controlled by clock input as seen in Houston's invention into the admitted prior art because they would enable to increase speed of calculation (e.g. col. 1 lines 40-42 based on the pre-charged of power and foot transistors).

Re claim 8, the admitted prior art fails to disclose in Figures 1-3 logic tree includes a plurality of transistor stacks, each transistor stack having a plurality of logic transistors serially connected source-to-drain, with one logic transistor in each stack having a source connected to drain of power transistor and dynamic node, and another logic transistor in each stack having a drain connected to source of foot transistor. However, Houston discloses in Figures 1-12 logic tree includes a plurality of transistor stacks (e.g. Figure 7 wherein there are 10 transistors total and three stacks of transistors), each transistor stack having a plurality of logic transistors serially connected source-to-

drain, with one logic transistor in each stack having a source connected to drain of power transistor and dynamic node, and another logic transistor in each stack having a drain connected to source of foot transistor (e.g. first column of the three stacks). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a logic tree includes a plurality of transistor stacks, each transistor stack having a plurality of logic transistors serially connected source-to-drain, with one logic transistor in each stack having a source connected to drain of power transistor and dynamic node, and another logic transistor in each stack having a drain connected to source of foot transistor as seen in Houston's invention into the admitted prior art because they would enable to increase speed of performing logic function (e.g. col. 1 lines 40-45 and col. 2 lines 65-66).

Re claim 9, the admitted prior art fails to disclose in Figures 1-3 a first source/drain junction in a first one of transistor stacks is connected to a second source/drain junction in a second one of transistor stacks. However, Houston discloses in Figures 1-12 a first source/drain junction in a first one of transistor stacks is connected to a second source/drain junction in a second one of transistor stacks (e.g. source of first column is connect to source of second column in Figure 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a first source/drain junction in a first one of transistor stacks is connected to a second source/drain junction in a second one of transistor stacks as seen in Houston's invention into the admitted prior art because they would enable to increase speed of performing logic function (e.g. col. 1 lines 40-45 and col. 2 lines 65-66).

Allowable Subject Matter

16. Claims 5-7 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,208,489* to Houston et al. disclose a multiple compound domino logic circuit.

b. U.S. Patent No. 6,393,446 to Dhong et al. disclose a 32-bit and 64-bit dual mode rotator.

c. U.S. Patent No. 6,393,454 to Chu discloses a booth multiplier with low power, high performance input circuity.

d. U.S. Patent No. 6,275,841 to Potter et al. disclose a 1-of-4 multiplier.

e. U.S. Patent No. 6,021,424 to Chu discloses a booth multiplier with low power, high performance input circuity.

f. U.S. Patent No. 7,024,445* to Qi discloses a method and apparatus for use in Booth-Encoded multiplication.

g. U.S. Patent No. 6,877,022 to Toyonoh et al. disclose a Booth encoding circuit for a multiplier of a multiply-accumulate module.

h. U.S. Patent No. 5,748,517 to Miyoshi et al. disclose a multiplier circuit.

i. U.S. Patent No. 5,040,139 to Tran discloses a transmission gate multiplexer (TGM) logic circuits and multiplier architectures.

j. U.S. Patent No. 5,773,995 to Crocker discloses a digital multiplexer circuit.

k. U.S. Patent No. 6,567,835* to Blomgren et al. disclose a method and apparatus for a 5:2 carry-save-adder (CSA).

l. U.S. Non-Patent Literature to Chris et al. disclose a timed circuits: a new paradigm for high-speed design.

m. U.S. Non-Patent Literature to Jaehong et al. disclose a 470ps 64bit parallel binary adder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 2, 2007